



PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Serial No.: 09/697,305

Confirmation No.: 4222

In re Application of:

Takaki YOSHIDA et al.

Group Art Unit: 2133

Filed: October 27, 2000

Examiner: Joseph D. Torres

For: FAULT DETECTING METHOD AND LAYOUT METHOD
FOR SEMICONDUCTOR INTEGRATED CIRCUIT

AMENDMENT

MAIL STOP AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

RECEIVED

AUG 31 2004

Technology Center 2100

Sir:

In response to the Office Action mailed May 26, 2004,
please amend the above-identified application as follows:

08/27/2004 EABUBAK1 00000023 09697305

01 FC:1201	430.00 OP
02 FC:1202	108.00 OP